Claims

2. (original) A method of storing and continuous looping transmission of digital HDTV signals comprising the steps of:

copying a first block of digital HDTV signals from 1 of 2 distinct blocks in a computer system memory to first in, first out registers,

identifying said first block of digital HDTV signals,

copying a second block of digital HDTV signals from the other of said two distinct blocks in a computer system memory to be the first in, first out registers,

identifying each of said distinct blocks of additional digital HDTV signals,

providing said constant flow of digital HDTV signals from said first in, first out registers to an 8-VSB modulator,

encoding said digital HDTV signals,

converting said digital HDTV signals into one of 8 voltage levels for providing a base band signal that is used to modulate a radio frequency carrier,

choosing one of said blocks of digital HDTV signals to be a start block and another one of said blocks of digital HDTV signals to be a finish block in a program to be transmitted,

playing said blocks of digital HDTV signals from said start block to said finish block,

continuously playing said blocks of digital HDTV signals in identified order with said start block positioned after said finish block in playing order.

3. (original) A method of re-clocking digital HDTV signals and preparing same for continuous looping play comprising:

filling two concurrent blocks of computer system memory with 32 bit wide digital HDTV signals and identifying the signals making up each distinct block thereof,

emptying one of said two concurrent blocks by a reading process,

emptying a second of said two concurrent blocks by a reading process while a microprocessor orders the refill of said first block at a faster rate than the emptying of said second block,

distributing said 32 bit wide digital HDTV signal across four 8 bit first in, first out registers by a bus master device via a bus,

dividing each first in, first out registers into two sections,

refilling each section as each register transitions a half full boundary, and

providing a constant predetermined rate and width digital HDTV signal sequentially in identifiable predetermined sized blocks of such signals from each of the four 8-bit first in, first out registers.